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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NG, CHRISTINE Y	

ART UNIT	PAPER NUMBER
2663	

DATE MAILED: 04/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/784,549	GUINEA ET AL.	
	Examiner	Art Unit	
	Christine Ng	2663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-30 and 32-35* is/are rejected.

7)☒ Claim(s) *31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 February 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 15 and 23 objected to because of the following informalities:

Both claims are the same.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 13, 14, 22, 24, 25, 32, 33 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,255,880 to Nguyen in view of U.S. Patent No. 4,419,629 to O'Brien.

Referring to claims 13, 22 and 32, Nguyen discloses in Figure 3 a switching circuit comprising at least one circuit (Delay line 305) for receiving a plurality of input clock signals (CLK0-CLKn) delayed relative to one another and at least one control signal (SELECT) and outputting a new signal (CLKOUT) from among the plurality of input clock signals (CLK0-CLKn) based upon the at least one control signal (SELECT), the new signal (CLKOUT) being advanced or delayed relative to a current signal from among the plurality of input signals (CLK0-CLKn) currently being output. Delay line 305 provides a plurality of clock signals CLK0-CLKn, delayed relative to one another by a unit delay, to clock

multiplexer 315, which then selects one of the clock signals as CLKOUT using the SELECT signal. Refer to Column 5, lines 4-47.

Nguyen does not disclose that the circuit outputting the new signal synchronously with a transition of the new signal and before disabling the current signal to substantially prevent the production of false signals during switching.

O'Brien discloses in Figure 1 a switching circuit with a plurality of clocks 11 and 12. Refer to Column 2, lines 11-14 and lines 56-63. The switching circuit selects one of a plurality of oscillators with a selection switch while the formerly selected oscillator is still working. The switching circuit then uses the output of the newly selected oscillator to disable the formerly selected oscillator. Refer to Abstract. This prevents a metastable condition which is "an attempt to change the state of a logic element before the elements has had time to become stable or enabled sufficiently to accept or sense the change signal" which may lead to an incorrect output. Refer to Column 1, lines 21-28. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include that the circuit outputs the new signal synchronously with a transition of the new signal and before disabling the current signal; the motivation being to prevent a metastable condition in which the desired output may be incorrect since the element has not had time to sense the change signal.

Referring to claim 14, Nguyen discloses in Figure 3 that the circuit (Delay line 305) comprises a plurality of circuits (Delay elements 306) each receiving a respective one of the plurality of input clock signals (CLK0-CLKn) and selectively outputting its respective input clock signal (CLK0-CLKn) as the new signal

(CLKOUT). Delay line 305 comprises delay elements 306 that store one of CLK0-CLKn. Refer to Column 5, lines 14-22.

Referring to claims 24 and 33, Nguyen discloses in Figure 3 that each of the input clock signals (CLK0-CLKn) is of equal period. The input clock signal is chosen from a plurality of delay stages 375, which have a delay of one unit delay, the same as in delay line 305. Refer to Column 5, line 57 to Column 6, line 20.

Referring to claims 25 and 34, Nguyen discloses in Figure 3 that the input clock signals are delayed equally relative to one another (by a unit delay) by a fraction equal to the period divided by a number of the plurality of circuits. Each delay element 306 provides an input clock signal one unit delay apart. Each unit delay is equal to a fraction of the period of GCLK. There are n intermediate clock signals each delayed by 0,1...n unit delays from the input clock signal GCLK, in order to align the FBCLK with GCLK. Refer to Column 4, lines 48-62 and Column 5, lines 14-22.

4. Claims 15-21, 23 and 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,255,880 to Nguyen in view of U.S. Patent No. 4,419,629 to O'Brien in view of U.S. Patent No. 6,091,705 to Regula and in further view of U.S. Patent No. 4,853,653 to Maher.

Referring to claim 15 and 23, Nguyen and O'Brien do not disclose that the plurality of circuits are connected in a ring.

Regula discloses in Figure 1a a ring network with a plurality of nodes 101, 103, 105 and 107 which each contain delay-locked loop circuitry. Refer to Column 6, lines 44-49, Column 9, lines 16-21 and Column 10, lines 27-34.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include that the plurality of circuits are connected in a ring; the motivation being that a ring network allows nodes to be connected together along the same signal path, thereby preventing collision of information since data transmission is unidirectional.

Nguyen, O'Brien and Regula also do not disclose that each of the plurality of circuits provides a respective disabling signal upon being selected to adjacent circuits in the ring to disable the adjacent circuits.

Maher discloses in Figure 1 a clock selector 10 that chooses one of oscillators f1, f2 or f3 to be the output clock signal. Each of the plurality of circuits (f1, f2 and f3) provides a respective disabling signal ($\bar{Q}$) upon being selected to adjacent circuits in the ring to disable the adjacent circuits. "The $\bar{Q}$ signal from each of the second flip-flops 16, 26 and 36, respectively, is fed back as an input to the initial AND gates in all of the sections of clock selector 10 other than its own" (Column 3, lines 6-9), in order to disable other clocks. For example, "the $\bar{Q}$ output of flip-flop 16 goes low and is input to AND gates 22 and 32 to "lock-out" f2 and f3..." (Column 3, lines 34-37). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include that each of the plurality of circuits provides a respective disabling signal upon being selected to adjacent circuits in the ring to disable the adjacent circuits; the motivation being to switch from one clock to another clock without "producing runt pulses or other anomalous signals during the switching

operation", such as metastable conditions. Refer to Column 1, lines 15-20 and Column 2, lines 51-54.

Referring to claim 16, Nguyen discloses in Figure 3 a decoding circuit (Decoder 380) for decoding the at least one control signal (SELECT), the decoding circuit (Decoder 380) providing at least one selection signal (SELECT) for activating one of the plurality of circuits based upon a state of the at least one control signal (SELECT). Decoder 380 supplies the select signals to clock multiplexer 315 to selector one of CLK0-CLKn. Refer to Column 5, line 45 to Column 6, line 21.

Referring to claim 17, refer to the rejection of claims 24 and 33.

Referring to claim 18, refer to the rejection of claims 25 and 34.

Referring to claims 19 and 26, Nguyen and O'Brien do not disclose that each disabling signal comprises a pulse, and that each of the plurality of circuits generates its respective pulse based upon the at least one selection signal.

Maher discloses in Figure 1 that the disabling signal ($\overline{Q}$) comprises a pulse, and that each of the plurality of circuits f1, f2 and f3 generates its respective pulse based upon a selection signal (SEL1, SEL2 or SEL3). For example, when SEL1 goes high, "the $\overline{Q}$ output of flip-flop 16 goes low and is input to AND gates 22 and 32 to "lock-out" oscillator signals f2 and f3" (Column 3, lines 26-37). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include that each disabling signal comprises a pulse, and that each of the plurality of circuits generates its respective pulse based upon the at least one selection signal; the motivation

being so that upon receiving the selection signal, the circuits that were not selected can be disabled, thereby preventing "runt pulses or other anomalous signals during the switching operation", such as metastable conditions. Refer to Column 1, lines 15-20 and Column 2, lines 51-54.

Referring to claims 20 and 27, Nguyen and O'Brien do not disclose that each of the plurality of circuits provides an enabling signal for enabling the transmission of its respective input clock signal based on the at least one selection signal, the enabling signal is activated synchronously with a trailing edge of the respective input clock signal.

Maher discloses in Figure 1 a plurality of circuits f1, f2 and f3 each providing an enabling signal (Q) for enabling the transmission of its respective input clock signal (f1, f2 or f3) based on the at least one selection signal (SEL1, SEL2 or SEL3), the enabling signal (Q) is activated synchronously with a trailing edge of the respective input clock signal (f1, f2 or f3). For example, when SEL2 goes high, "the Q output of flip-flop 24 goes high on the next falling edge of oscillator signal f2. Thereafter, the Q output of flip-flop 2 goes high and the Q output goes low on the second falling edge of oscillator signal f2". Refer to Column 3, lines 48-63. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include that each of the plurality of circuits provides an enabling signal for enabling the transmission of its respective input clock signal based on the at least one selection signal, the enabling signal is activated synchronously with a trailing edge of the respective input clock signal; the motivation being that upon receiving the selection signal,

the circuit that was selected can be enabled, thereby preventing "runt pulses or other anomalous signals during the switching operation", such as metastable conditions. Refer to Column 1, lines 15-20 and Column 2, lines 51-54. The enabling signal is also activated synchronously with the trailing edge of the input clock signal since it is stored in an edge-triggered flip-flop so that it can be stored and change states based on the clock as a triggering input.

Referring to claims 21 and 28, Nguyen and O'Brien do not disclose that each of the plurality of circuits deactivates its respective enabling signal upon receiving the disabling signal.

Maher discloses in Figure 1 a plurality of circuits f1, f2 and f3 that can deactivate its respective enabling signal (Q) when receiving a disabling signal ($\overline{Q}$). For example, when SEL1 goes high, "the $\overline{Q}$ output of flip-flop 16 goes low and is input to AND gates 22 and 32 to "lock-out" oscillator signals f2 and f3" (Column 3, lines 26-37). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include that each of the plurality of circuits deactivates its respective enabling signal upon receiving the disabling signal; the motivation being so that upon receiving the selection signal, the circuits that were not selected can be disabled, thereby preventing "runt pulses or other anomalous signals during the switching operation", such as metastable conditions. Refer to Column 1, lines 15-20 and Column 2, lines 51-54.

5. Claims 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,255,880 to Nguyen in view of U.S. Patent

No. 5,022,056 to Henderson et al, and in further view of U.S. Patent No. 4,419,629 to O'Brien.

Referring to claim 29, Nguyen discloses in Figure 3 a circuit for recovering data from a serial data flow comprising:

A generator (Delay line 305) for generating a plurality of clock signals (CLK0-CLKn) of equal period that are delayed equally relative to one another by a fraction equal to the period divided by a number of the plurality of clock signals. Refer to the rejection of claims 24, 25, 33 and 34.

A switching circuit (Clock mux 315) for receiving the plurality of clock signals (CLK0-CLKn) and providing one of the clock signals (CLKOUT) as an output thereof. Clock multiplexer selects one of CLK0-CLKn and provides the selcted signal as signal CLKOUT. Refer to Column 5, lines 4-8.

A phase comparator (Mux Control 350) for receiving the output (CLKOUT) from the switching circuit (Clock mux 315) and a global clock (GCLK) and providing at least one phase difference signal indicating a phase difference therebetween. Mux Control 350 chooses a clock signal CLK0-CLKn in order to adjust for the phase difference between CLKOUT and GCLK. Refer to Column 5, lines 32-47.

A controller (Decoder 380) for receiving the at least one phase difference signal from the phase comparator (Mux control 350) and controlling the switching circuit (Clock mux 315) based thereon to switch the output of the switching circuit (Clock mux 315) to one of the clock signals providing a smaller phase difference than a current clock signal. Mux control 350 determines the amount of unit

delays needed to delay the CLKOUT signal to bring it back into synchronization with the GCLK signal; decoder 380 uses this information to provide clock multiplexer 315 with the correct clock signal. Refer to Column 5, lines 32-47.

Nguyen does not disclose that the input clock signals are compared with a data flow signal comprising a flow of data.

Henderson et al discloses in Figure 5 that a plurality of input clock signals 503-1 to 503-N provide delayed versions of the clock signals and are compared with a data flow 501 to determine which is the delayed clock signal is closest in phase to the receiver input signal. Refer to Column 4, lines 7-23 and Abstract. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the input clock signals are compared with a data flow signal comprising a flow of data; the motivation being to synchronize a received data stream to the receiver clock in order to recover the received data accurately. Refer to Column 1, lines 18-28 and lines 59-61.

Nguyen does not disclose that the switching circuit (Clock mux 315) providing the output synchronously with a transition of the output and before disabling a current output to substantially prevent the production of false signal during switching. Refer to the rejection of claim 13.

Referring to claim 30, Nguyen does not specifically disclose that the generator comprises a delay-locked loop circuit. However, Nguyen discloses a delay-locked loop circuit 301. Delay-locked loop circuits require "many input clock cycles to "lock", i.e., to synchronize a destination clock signal to an input clock signal" (Column 1, lines 50-60). Therefore, it would have been obvious to

one of ordinary skill in the art at the time the invention was made to include that the generator comprises a delay-locked loop circuit; the motivation being that a delay-lock loop provides a method to synchronize an incoming clock signal to a destination clock signal; thereby allowing the accurate recovery of data.

6. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,255,880 to Nguyen in view of U.S. Patent No. 4,419,629 to O'Brien, and in further view of U.S. Patent No. 4,853,653 to Maher. Refer to the rejection of claims 20 and 27.

Allowable Subject Matter

7. Claim 31 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

8. Applicant's arguments filed December 9, 2004 have been fully considered but they are not persuasive.

Referring to the argument that O'Brien teaches outputting the new signal after disabling the current signal (page 12, line 3 to page 13, line 2), refer to Figure 1. O'Brien discloses that the "switching circuit employs the output of the newly selected oscillator to disable the formerly selected oscillator..." (abstract, lines 5-7). Therefore, the new signal is outputted before disabling the current signal, since it is used to disable the current signal. Furthermore, O'Brien discloses that when a new oscillator N is chosen, "switch selection means presents a select signal on line 19 to set the new select storage element 20

which generates a new oscillator selection output signal on line 21".... the "old oscillator select element 22 still retains the previous selected oscillator 11 and is presenting a high output on line 23" (Column 3, lines 15-21). "When line 21 goes high, the high output of line 21 is presented to the AND gate 24 along with the output of oscillator 12 causing a high output at AND gate 24..." (Column 3, lines 21-24). Again, the new signal (from oscillator N) is outputted (on line 21) before the old signal (from oscillator 11) is disabled (on line 23).

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christine Ng whose telephone number is (571) 272-3124. The examiner can normally be reached on M-F; 8:00 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on (571) 272-3139. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C. Ng CN
April 7, 2005

RICKY NGO
PRIMARY EXAMINER

3/11/05